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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/592,009	06/12/2000	Sherman Lee	M-8815 US	4198	
23363 75	90 11/02/2006		EXAMINER		
CHRISTIE, PARKER & HALE, LLP			NGUYEN, TANH Q		
PO BOX 7068 PASADENA, CA 91109-7068			ART UNIT	PAPER NUMBER	
,			2182		
			DATE MAILED: 11/02/2006	DATE MAILED: 11/02/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
·	09/592,009	LEE ET AL.			
Office Action Summary	Examiner	Art Unit			
	Tanh Q. Nguyen	2182			
The MAILING DATE of this communication		1			
Period for Reply					
A SHORTENED STATUTORY PERIOD FOR RE WHICHEVER IS LONGER, FROM THE MAILING  - Extensions of time may be available under the provisions of 37 CFF after SIX (6) MONTHS from the mailing date of this communication  - If NO period for reply is specified above, the maximum statutory pe  - Failure to reply within the set or extended period for reply will, by st. Any reply received by the Office later than three months after the m earned patent term adjustment. See 37 CFR 1.704(b).	B DATE OF THIS COMMUNIC R 1.136(a). In no event, however, may a re- riod will apply and will expire SIX (6) MON atute, cause the application to become AB.	CATION.  Sply be timely filed  THS from the mailing date of this communication.  ANDONED (35 U.S.C. § 133).			
Status					
1)⊠ Responsive to communication(s) filed on 2	8 September 2006				
	This action is non-final.				
· <u> </u>	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is				
closed in accordance with the practice unde		-			
Disposition of Claims					
4)⊠ Claim(s) <u>1-13</u> is/are pending in the applicat	ion				
4a) Of the above claim(s) is/are without		•			
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-13</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction an	d/or election requirement.				
Application Papers					
9)☐ The specification is objected to by the Exam	inor	•			
10)⊠ The drawing(s) filed on 12/02/05 is/are: a)		a by the Everiner			
Applicant may not request that any objection to the	• • •	•			
Replacement drawing sheet(s) including the con-					
11) The oath or declaration is objected to by the		·			
Priority under 35 U.S.C. § 119	Examinor. Note the attached	5/105 / total of 10/1/17   10-102.			
<u> </u>					
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of:	ign priority under 35 U.S.C. §	119(a)-(d) or (f).			
	anta haya haan raasiyad				
<ul> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> </ul>					
3. ☐ Copies of the certified copies of the p		· · · · · · · · · · · · · · · · · · ·			
application from the International Burn		eceived in this National Stage			
* See the attached detailed Office action for a l	. , ,	ereived			
See and small designed children design for de	is and sommed supres flot in				
Attachment(s)	_				
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948)		ımmary (PTO-413) /Mail Date			
B) Information Disclosure Statement(s) (PTO/SB/08)	5) 🔲 Notice of Inf	formal Patent Application			
Paper No(s)/Mail Date	6)  Other:				

#### **DETAILED ACTION**

#### Status of Claims

1. The examiner notes that applicant did not appear to take into consideration the examiner's amendment in the Notice of Allowability mailed September 15, 2005 - which amended claims 1 and 8 and canceled claim 14. Accordingly, claim 14 is considered canceled by the examiner. The examiner would take both the examiner's amendment and the amendment filed September 28, 2006 into consideration for this office action. For subsequent actions, applicant needs to make sure the claims are correctly represented.

### Election/Restrictions

2. Newly submitted claims 15-20 are directed to an invention (Invention III) that is independent or distinct from the inventions originally claimed (Inventions I and II) for the following reasons:

Invention I (claims 1-7) and Invention III (claims 15-20) are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another and materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case, the process of Invention I can be practiced on a peripheral system that does not require a host controller comprising a state machine, the state machine comprising a first register storing information corresponding to a wireless device, and a control logic performing

one of read operation and a write operation with respect to the first register associated with a data value loaded into a second register.

Invention II (claims 8-13) and Invention III (claims 15-20) are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination includes a host computer that interacts with the peripheral system. The subcombination has separate utility such as a host controller and a state machine, the state machine comprising a first register storing information corresponding to a wireless device, and a control logic performing one of read operation and a write operation with respect to the first register associated with a data value loaded into a second register.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 15-20 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance

with 37 CFR 1.67(a) identifying this application, by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

Page 4

The oath or declaration is defective because it does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

## Claim Objections

4. Claim 6 is objected to because of the following informalities: "accessing context data" in line 1 should be replaced with "accessing context data in a second register" to be in concordance with line 4 of the claim.

### Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

Art Unit: 2182

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

- 7. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin et al. (USP 6,154,832).
- 8. <u>As per claim 1</u>, Maupin teaches a method for performing a context switch operation, comprising:

accessing context data in a first register [a first one of 46A-46H, FIG. 2] of a peripheral system [embedded controller 10, FIG. 1] when a context index register [42, FIG. 2] is set to a first index value [col. 6, lines 20-29];

receiving by the peripheral system a second index value from an external interrupt source associated with the peripheral system [col. 6, lines 20-29];

setting the context index register to the second index value to perform a context switch by accessing context data in a second register [a second one of 46A-46H, FIG. 2] of the peripheral system when the context index register is set to the second index value [FIG. 5; col. 7, line 63-col. 8, line 8], wherein the first and second registers are collocated with the peripheral system [the registers are collocated on embedded controller 10, FIG. 1].

Maupin, therefore teaches the invention except for the external interrupt source being a host computer. Since it was known in the art at the time the invention was made for an interrupt source of an embedded controller to be a host computer in order

Page 6

Art Unit: 2182

to allow the host computer to request service from the embedded controller, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the interrupt source of the peripheral system to be a host computer in order to allow the host computer to request service from the peripheral system.

9. As per claim 2, Maupin does not teach context data including a device address for a network device, a class value, a clock offset value and an active member address. Such context data are traditionally associated with communications in a Bluetooth environment.

Maupin in essence teaches reducing or eliminating the need for context save and restore when performing context switch operations - by using register sets, each of which being dedicated to a particular context [col. 4, lines 24-36]. Maupin, however, does not teach a Bluetooth environment.

Since it was known in the art at the time the invention was made that traditional context switch operations in a Bluetooth environment require substantial context save and restore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate registers, each of which being dedicated to a particular context (as is taught by Maupin) in a Bluetooth environment - in order to reduce and/or eliminate context save and restore when performing context switch operations in such environment (hence context data in such environment including a device address for a network device, a class value, a clock offset value and an active member address)

10. As per claims 3-6, Maupin teaches each register being dedicated to a task

Art Unit: 2182

context data comprising receiving by the peripheral system an address value that identifies an address within the register, control input identifying read/write functions, and data value to write the data value to the register for a write function, or to provide the contents of the register to the interrupt source for a read function - as read/write interrupts are known to include address, read/write functions and data value for write functions.

Page 7

- 11. <u>As per claim 7</u>, Maupin teaches the registers [46A-46H, FIG. 2] being dedicated to particular contexts hence the first and second registers not being architected registers.
- 12. <u>As per claim 8, Maupin teaches a system [FIG. 1] comprising:</u>

a peripheral system [10, FIG. 1] coupled to an interrupt source, the peripheral system including a first register and a second register, the first register being associated with a first index value and the second register being associated with a second index value [see rejection of claim 1 above], wherein the first and second registers are collocated with the peripheral system [the registers are collocated on embedded controller 10, FIG. 1];

an interface [14, FIG. 1] coupled to the interrupt source and to the peripheral system, the interface being configured to provide first and second index values from the interrupt source to the peripheral system [col. 4, lines 24-28]; and

a register access circuit [40, 42, FIG. 2] coupled to the interrupt source, the register access circuit being configured to access context data in the first register if the

first index value is provided by the interrupt source, and the register access circuit being configured to access context data in the second register if the second index value is provided by the interrupt source [see rejection of claim 1 above],

wherein the peripheral system includes a context index register [42, FIG. 2] for storing the first and second index values [see rejection of claim 1 above].

Maupin, therefore teaches the invention except for the external interrupt source being a host computer including a microprocessor. Since it was known in the art at the time the invention was made for an interrupt source of an embedded controller to be a host computer (that inherently includes a microprocessor) in order to allow the host computer to request service from the embedded controller, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the interrupt source of the peripheral system to be a host computer in order to allow the host computer to request service from the peripheral system.

13. As per claims 9-13, Maupin teaches the registers [46A-46H, FIG. 2] being dedicated to particular contexts - hence the first and second registers not being architected registers;

the peripheral system including a state machine module [40, 42, 44, FIG. 2] that includes an address portion, a control portion, and a data portion (execution core 40 inherently comprising address portion, control portion and data portion), the data portion including the first and second registers [46A-46H included in register file 44, FIG. 2];

the peripheral system including a microprocessor [12, FIG. 1]; the address portion comprising the register access circuit [40, 42, FIG. 2];

the peripheral system including a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values [8 register sets 46A-46H corresponding to 8 index values].

# **Double Patenting**

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 1-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-5 of copending Application No. 11/314,036 in view of Maupin.

As per claims 1, 8, 13, claims 1, 5 of the copending application claim all the limitations of the claims except for a context index register for setting the index values.

Art Unit: 2182

Maupin teaches a context index register for setting a value identifying a new context in a context switch operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a context index register, as is taught by Maupin, in order to identify a new context in a context switch operation.

As per claims 2-6, claim 5 of the copending application claims a Bluetooth network and communications in a Bluetooth network, hence the context data of claim 2, and accessing the context data of claims 3-6.

As per claims 7, 9, claim 4 of the copending application claims non-architected registers.

As per claims 10-12, claim 5 of the copending application claims a host controller, hence a state machine, a microprocessor and a register access circuit in the host controller.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

## Response to Arguments

16. Applicant's arguments have been considered but are either moot in view of the new ground(s) of rejection or not persuasive.

Applicant argued that the processor 12 in FIG. 1 and in FIG. 2 of Maupin is the host computer and the registers are collocated with processor 12. The argument is not persuasive because it is misplaced. The examiner considers the peripheral system to be embedded controller 10, and the host computer to be external to the embedded

controller. The registers are therefore collocated with the peripheral system.

#### Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Art Unit: 2182

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TANH Q NGUYEN
PRIMARY EXAMINER
TECHNOLOGY CENTER-2100

Page 12

TQN October 28, 2006